Computer Architecture Lab 08

Memory System and Address Decoding – Instruction/Data Access

Introduction

This lab is intended as an exercise in integrating memory systems (instruction and data memory) into your processor, and implementing a system of address decoding to access data and I/O memory outside the processor.

Objectives

* To understand and implement memory systems in a processor design.
* To integrate instruction memory (ROM) for storing and fetching RISC-V instructions.
* To implement data memory (RAM) for performing load and store operations.
* To design and implement address decoding logic that differentiates between data memory, and I/O regions (such as LEDs and buttons).
* To verify correct memory access by reading and writing data, and displaying the results using LEDs.

Sections

|  |  |
| --- | --- |
| Section |  |
| a) Task 1 | **40** |
| You will learn how to take button input to change the state of internal variables. |
|  |
| c) Task 2: | **40** |
| In this section, you will develop modules to write outputs to output peripherals such as Seven Segment LED on the FPGA. |
|  |
| d) Task 3: | **100** |
| In this section, you will develop a counter with user-configurable delay values. |
|  |

Task 1: Data Memory